WHAT IS CLAIMED IS:

1. A method for improved digital communications, comprising:

receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

slicing a chip from the encoded symbol;

removing interference from the chip;

deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word; and

providing the more accurate symbol estimate as input to the chip slicer.

2. The method of claim 1, wherein the receiving step further comprises receiving the encoded symbol during the data portion of a frame.

3. The method of claim 2, wherein the providing step comprises decision directed updating during the data portion of a frame.

4. The method of claim 1, wherein at least fifty percent of the symbol estimates provided to the chip slicer are more accurate.

5. The method of claim 1, further comprising:

providing the more accurate symbol estimate to the feedback filter; and

storing the more accurate symbol estimate in the feedback filter.

6. The method of claim 5, where in the removing step further comprises using the more accurate symbol estimate stored in the feedback filter for improved performance in removing interference from the chip.

7. The method of claim 5, wherein at least fifty percent of the symbol estimates stored in the feedback filter are more accurate.

8. The method of claim 1, wherein the method is repeated to create more reliable symbol estimates relative to older symbol estimates already derived, and wherein the more reliable symbol estimates are used in a feedback filter to improve the accuracy of the symbol estimates being fed into the chip slicer.

9. A system for improved digital communications, comprising:

a chip slicer for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream;

a feed back filter configured to remove interference from sliced chips, the feedback filter having a plurality of content registers; and

a chip combiner configured to derive a more accurate symbol estimate for a sliced chip, wherein the chip combiner provides improved symbol estimates to the chip slicer.

10. The system of claim 9, wherein one or more content registers are updated with more accurate symbol estimates during decision directed updating.

11. The system of claim 10, wherein the majority of the plurality of content registers contain more accurate symbol estimates.

12. The system of claim 9, wherein the feed back filter is a finite impulse response ("FIR") filter, wherein the FIR subtracts out postcursor inter-symbol interference from the current slicer input.

13. The system of claim 9, wherein the chip combiner derives a more accurate symbol estimate based on a correlation among the chips in the code word.

14. A receiver for use in a block coded digital communications system, comprising:

a preprocessor for carrying out signal processing tasks and for providing a feed forward filter with baseband samples;

the feed forward filter for processing the baseband samples and for sending a digital data stream to a chip slicer in combination with any signal added or subtracted by a chip combiner; and

a feedback filter for processing previous chip slicer outputs to subtract out postcurser inter symbol interference from the current input to the chip slicer.

15. The receiver of claim 14, wherein coefficients for the feed forward filter and the feedback filter are selected based on minimum mean square error (MMSE) criterion using either adaptive techniques or based on computations involving a channel estimate.

16. The receiver of claim 14, wherein the chip slicer is configured to extract a portion of the data stream that corresponds to a single chip of a code word.

17. The receiver of claim 14, wherein the feedback filter feeds the noise component back into the chip slicer by way of a chip combiner so that the noise component can be subtracted from the next incoming signal from the feed forward filter before the next incoming signal is fed into the chip slicer.

18. A receiver for use in a block coded digital communications system, comprising:

means for receiving a frame in a digital communications stream, the frame having a training portion and a data portion, wherein the data portion comprises an encoded symbol, the encoded symbol having a plurality of code words, wherein each code word has a plurality of chips;

means for slicing a chip from the encoded symbol;

means for removing interference from the chip;

means for deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word; and

means for providing the more accurate symbol estimate as input to the chip slicer.

19. The receiver of claim 18, wherein the means for slicing a chip from the encoded symbol further comprises a chip slicer for extracting a chip from a code word, the code word received as part of an encoded symbol in a digital communication stream.

20. The receiver of Claim 19, wherein the means for removing interference from the chip further comprising a feed back filter configured to remove interference from sliced chips, the feed back filter having a plurality of content registers.

21. The receiver of claim 20, wherein the means for deriving a more accurate symbol estimate for the sliced chip based on a correlation among the chips in the code word further comprises a chip combiner configured to derive a more accurate symbol estimate for a sliced chip, and wherein the chip combiner provides improved symbol estimates to the chip slicer.